AMENDMENTS TO THE CLAIMS:

Claims 1-9 (Cancelled)

10. (New) A decoding apparatus comprising:

an input terminal that receives a compressed input signal including a data signal:

a demultiplexer that separates the data signal from the input signal;

a decoder buffer that stores a compressed video signal and a compressed audio signal;

a video decoder that decodes the compressed video signal stored in the decoder buffer;

an audio decoder that decodes the compressed audio signal stored in the decoder buffer;

a memory that stores the data signal separated by the demultiplexer; and

a CPU that analyzes the data signal stored in the memory;

wherein the CPU allows the data signal analyzed by the CPU to be stored in the decoder buffer if the analyzed data signal includes a compressed video signal or a compressed audio signal, and the compression method used for the compressed video signal or the compressed audio signal included in the data signal can be decoded by the video decoder or the audio decoder.

11. (New) The decoding apparatus of claim 10, wherein said CPU decodes the analyzed data signal if the compression method used for the compressed video signal or the compressed audio signal included in the data signal cannot be decoded by the video decoder or the audio decoder.

12. (New) The decoding apparatus of claim 10, wherein said decoder buffer stores the compressed video signal and the compressed audio signal, as well as a compressed video signal or a compressed audio signal that may be included in the data signal, using time division.

13. (New) The decoding apparatus of claim 10, wherein said video decoder and said audio decoder retain a write address used when a compressed video signal or a compressed audio signal included in said data signal is stored in said decoder buffer, and determine the progress of decoding or determine whether the compressed video signal or the compressed audio signal in the decoder buffer is depleted, based on a difference between the write address and the read address for said video decoder and said audio decoder to read said decoder buffer, whereby said video decoder and said audio decoder stop, resume, or repeat decoding.

14. (New) The decoding apparatus of claim 10, wherein said video decoder and said audio decoder produce an interrupt signal for said CPU according to whether the compressed video signal and the compressed audio signal in said decoder buffer are depleted or not, or according to the progress of decoding, whereby said CPU controls decoding in response to said interrupt signal.

15. (New) The decoding apparatus of claim 10, wherein said video decoder and said audio decoder produce a frame pulse interrupt signal for said CPU, whereby said CPU receives said frame pulse interrupt signal and controls decoding by counting the number of frames related to frames of said compressed video signal and said compressed audio signal.

16. (New) A receiver comprising:

an input terminal for receiving a compressed input signal including a data signal;

a demultiplexer for separating the data signal from the input signal;

a decoder buffer for storing a compressed video signal and a compressed audio signal;

a video decoder for decoding said compressed video signal stored in said decoder buffer;

a display for displaying a video signal decoded by said video decoder;

an audio decoder for decoding said compressed audio signal stored in said decoder buffer;

a speaker for outputting an audio signal decoded by said audio decoder;

a memory for storing said data signal separated by said demultiplexer; and

a CPU for analyzing the data signal stored in said memory;

wherein said CPU allows the data signal analyzed by said CPU to be stored in said decoder buffer if the analyzed data signal includes a compressed video signal or a compressed audio signal, and the compression method used for the compressed video signal or the compressed audio signal included in the data signal can be decoded by the video decoder or the audio decoder.

17. (New) A CPU for receiving and processing a compressed input signal including a data signal, wherein:

said CPU determines whether a compressed video signal or a compressed audio signal is included in said data signal, and determines the compression method used for the compressed video signal or the compressed audio signal included in the data signal; and

based on the result of the determinations, said CPU changes the destination to which the data signal is outputted.

18. (New) The CPU of claim 17, wherein:

if the CPU determines that that the decompression method used for a compressed video signal or a compressed audio signal included in the data signal can be decoded by a video decoder or a audio decoder, the CPU causes the data signal to be stored in a decoder buffer to be decoded by the video decoder or the audio decoder, and

if the CPU determines that the compression method used for the compressed video signal or the compressed audio signal included in the data signal cannot be decoded by the video decoder or the audio decoder, the CPU decodes the data signal.

19. (New) A decoder for receiving and processing a compressed input signal including a data signal comprising:

a decoder buffer for storing a compressed video signal and a compressed audio signal;

a video decoder for decoding said compressed video signal stored in said decoder buffer;

an audio decoder for decoding said compressed audio signal stored in said decoder buffer; and

a CPU for analyzing said data signal,

wherein said CPU allows the data signal analyzed by said CPU to be stored in said decoder buffer if the analyzed data signal includes a compressed video signal or a compressed audio signal, and the compression method used for the compressed video signal or the compressed audio signal included in the data signal can be decoded by the video decoder or the audio decoder.

20. (New) A signal receiver comprising:

a demultiplexer configured to receive a compressed input signal and separate a data signal from the input signal;

a decoder buffer coupled to the demultiplexer to store a compressed video signal and a compressed audio signal;

a video decoder coupled to the decoder buffer to receive and decode the compressed video signal;

an audio decoder coupled to the decoder buffer to receive and decode the compressed audio signal;

a memory coupled to the demultiplexer to receive and store the data signal; and

a CPU coupled to the memory to receive and analyze the data signal stored in the memory;

wherein if the data signal includes a compressed video signal or a compressed audio signal that is compressed using a compression method that can be decoded by the video decoder or the audio decoder, the CPU causes the data signal to be stored in the decoder buffer to enable processing of the data signal by at least one of the decoders.

21. (New) The signal receiver according to claim 20, wherein the CPU decodes the data signal in response to the data signal not containing data that is compressed using a compression method that can be decoded by the video decoder or the audio decoder.

22. (New) The signal receiver according to claim 20, wherein the decoder buffer is configured to store the compressed video signal and the compressed audio signal, as well as a

compressed video signal or a compressed audio signal that may be included in the data signal, using time division.

23. (New) The signal receiver according to claim 20, wherein the video decoder and the audio decoder retain a write address used when a compressed video signal or a compressed audio signal included in the data signal is written into the decoder buffer, and determine the progress of decoding or determine whether the compressed video signal or the compressed audio signal in the decoder buffer is depleted, based on a difference between the write address and a read address for the video decoder and the audio decoder to read the decoder buffer, whereby the video decoder and the audio decoder stop, resume, or repeat decoding of data.

24. (New) The signal receiver according to claim 20, wherein the video decoder and the audio decoder produce an interrupt signal for the CPU according to whether the compressed video signal and the compressed audio signal in the decoder buffer are depleted, or according to the progress of decoding, whereby the CPU controls decoding data based on the interrupt signal.

25. (New) The signal receiver as claimed in claim 20, wherein the video decoder and the audio decoder produce a frame pulse interrupt signal, whereby the CPU, responsive to the frame pulse interrupt signal, controls decoding compressed video signals or compressed audio signals by counting the number of frames related to frames of the compressed video signals and the compressed audio signals.